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APPLICATION FOR LETTERS PATENT

Title : SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims priority of Japanese Patent Application Nos. 2001-059060, filed on March 2, 2001 and 2002-024468, filed on January 31, 2002, the contents being incorporated herein by reference.

BACKGROUND OF THE INVENTION

[Field of the Invention]

The present invention relates to a method of manufacturing a semiconductor device and, more specifically, is preferably applied to the formation of a source and a drain in a MOS transistor of a generation having a gate length of less than 0.1 μm.

[Description of the Related Art]

In recent years, the laser annealing technique is expected as thermal process of the next generation, replacing rapid lamp heating. This technique, nonequilibrium thermal process which is a melting and re-crystallization process in a very short period of time of several nanoseconds, has advantages in its capability of obtaining high electrical activity exceeding the solubility limit of impurities in a semiconductor which is normally limited by temperature and, further, of obtaining a sharp impurity profile. Therefore, this technique enables the formation of a source and a drain having a low

contact resistance and shallower and sharper impurity extension regions.

However, the sharp impurity extension obtained by the laser annealing has a disadvantage in that the impurity extension region in the vicinity of a gate electrode which is a mask during ion implantation is strictly defined because the impurity profile is too sharp, which inversely increases its parasitic resistance.

As described above, the use of the laser annealing method provides this sharp impurity profile due to the activating process in a very short period of time which greatly contributes to a reduction in the contact resistance and so on, but conversely presents a serious problem in the increase in parasitic resistance.

SUMMARY OF THE INVENTION

Therefore, the present invention is made in view of the aforementioned problem, and it is an object of the invention to provide a semiconductor device and a method of manufacturing thereof capable of making it possible to obtain a sharp impurity profile through the use of the laser annealing method without presenting a disadvantage such as an increase in parasitic resistance or the like, so as to make it possible to meet sufficiently the requirements for

making a semiconductor element finer and more highly integrated.

As a result of intense consideration, the present inventor achieved the aspects of the invention shown as follows:

The manufacturing method of the present invention (first aspect) is for a method of manufacturing a semiconductor device having a gate, a source and a drain within a single crystal semiconductor region, including: a first step of pattern forming the gate above the single crystal semiconductor region through a gate insulating film; a second step of introducing atoms having properties just enough to amorphize the single crystal semiconductor from oblique directions to a surface of the single crystal semiconductor region with the gate as a mask to form amorphous regions seeping into the single crystal semiconductor region under the gate; before or after the second step, a third step of introducing impurities into the surface of the single crystal semiconductor region with the gate as a mask; and a fourth step of activating the impurities by executing laser irradiation on the single crystal semiconductor region to form the source and the drain.

Further, the invention (second aspect) is for a method of manufacturing a semiconductor device of a so-called LDD structure, including: a first step of pattern forming the gate above the single crystal

semiconductor region through a gate insulating film; a second step of introducing atoms having properties just enough to amorphize the single crystal semiconductor from oblique directions to a surface of the single crystal semiconductor region with the gate as a mask to form first amorphous regions seeping into the single crystal semiconductor region under the gate; before or after the second step, a third step of introducing impurities into the surface of the single crystal semiconductor region with the gate as a mask to form first junction regions; a fourth step of forming a side wall insulating film on side surfaces of the gate; a fifth step of introducing atoms having properties just enough to amorphize the single crystal semiconductor into the surface of the single crystal semiconductor region with the gate and the side wall insulating film as a mask to form second amorphous regions which are deeper than the first amorphous regions; before or after the fifth step, a sixth step of introducing impurities into the surface of the single crystal semiconductor region with the gate and the side wall insulating film as a mask to form second junction regions which are deeper than the first junction regions; and a seventh step of removing the side wall insulating film and thereafter activating the impurities in the first and second junction regions by executing laser

irradiation on the single crystal semiconductor region to form the source and the drain.

Further, a method of manufacturing a semiconductor device of the present invention (third aspect) includes the steps of: introducing atoms having properties just enough to amorphize a single crystal semiconductor using a predetermined mask at least twice under different introduction conditions to form each amorphous region having a different depth and area in accordance with each introduction of the atoms; introducing impurities for forming a pn junction before or after each introduction of the atoms; and activating the introduced impurities by executing laser irradiation on the single crystal semiconductor region to form the pn junction.

Further, a method of manufacturing a semiconductor of the present invention (fourth aspect) includes: a first step of pattern forming the gate above the single crystal semiconductor region through a gate insulating film; a second step of introducing atoms having properties to amorphize the single crystal semiconductor into a surface of the single crystal semiconductor region with the gate as a mask to form amorphous regions; before or after the second step, a third step of introducing impurities into the surface of the single crystal semiconductor region with the gate as a mask; and a fourth step of activating the impurities by executing laser

irradiation on the single crystal semiconductor region to form the source and the drain, wherein conditions of introducing the atoms in the second step and conditions of intensity of the laser irradiation in the fourth step are controlled respectively to form parts of the source and the drain corresponding to the amorphous regions to seep into the single crystal semiconductor region under the gate.

Further, a method of manufacturing a semiconductor of the present invention (fifth aspect) includes: a first step of pattern forming the gate above the single crystal semiconductor region through a gate insulating film; a second step of forming a side wall insulating film on side surfaces of the gate and introducing impurities to form deep, first junction regions; a third step of removing the side wall insulating film and thereafter introducing atoms having properties just enough to amorphize the single crystal semiconductor into a surface of the single crystal semiconductor region with the gate as a mask to form amorphous regions; before or after the second step, a fourth step of introducing impurities into the surface of the single crystal semiconductor region with the gate as a mask to form shallow, second junction regions; and a fifth step of activating the impurities in the first and second junction regions by executing laser irradiation on

the single crystal semiconductor region to form the source and the drain, wherein conditions of introducing the atoms in the third step and conditions of intensity of the laser irradiation in the fifth step are controlled respectively to form parts of the source and the drain corresponding to the amorphous regions to seep into the single crystal semiconductor region under the gate.

Further, a method of manufacturing a semiconductor of the present invention (sixth aspect) includes: a first step of pattern forming the gate above the single crystal semiconductor region through a gate insulating film; a second step of introducing atoms having properties just enough to amorphize the single crystal semiconductor from oblique directions to a surface of the single crystal semiconductor region with the gate as a mask to form amorphous regions seeping into the single crystal semiconductor region under the gate; before or after the second step, a third step of introducing impurities into the surface of the single crystal semiconductor region with the gate as a mask; and a fourth step of activating the impurities by executing laser irradiation on the single crystal semiconductor region to form the source and the drain, wherein in the second step, tilt angles of the introduction of the atoms with respect to a direction vertical to the surface of the single crystal semiconductor region

are controlled to be greater on the source side than on the drain side so as to form the amorphous regions such that an amount of seeping into the single crystal semiconductor region under the gate is greater on the source side than on the drain side.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view illustrating manufacturing process of a MOS transistor for explaining a main configuration of the present invention;

Fig. 2 is a characteristic diagram showing results of secondary ion mass spectrometry of samples to which Ge implantation and B implantation are executed and then laser annealing is performed;

Fig. 3 is a schematic cross-sectional view illustrating manufacturing process of a MOS transistor for explaining another main configuration of the present invention;

Fig. 4 is a characteristic diagram showing the relationship between the laser power and the overlapping length between a lower part of a gate electrode, and a source and a drain;

Figs. 5A to 5E are schematic cross-sectional views illustrating in order of step a method of manufacturing a MOS transistor according to a first embodiment of the present invention;

Figs. 6A to 6C are schematic cross-sectional views illustrating in order of step the method of manufacturing the MOS transistor subsequent to Fig. 5E according to the embodiment of the present invention;

Figs. 7A to 7D are schematic cross-sectional views illustrating in order of step a method of manufacturing of a MOS transistor according to a second embodiment of the present invention;

Figs. 8A to 8D are schematic cross-sectional views illustrating in order of step a method of manufacturing a MOS transistor according to a third embodiment of the present invention;

Figs. 9A to 9E are schematic cross-sectional views illustrating in order of step a manufacturing method of a modified example 1 of a MOS transistor according to the third embodiment of the present invention; and

Figs. 10A to 10E are schematic cross-sectional views illustrating in order of step a manufacturing method of a modified example 2 of a MOS transistor according to the third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereafter, concrete embodiments of a method of manufacturing a semiconductor device to which the

present invention is applied will be described in detail with reference to the drawings.

-Main principle of the present invention-

At the beginning, the main principle of the present invention is explained by illustrating the case in which the present invention is applied to manufacturing of a MOS transistor including a gate, a source and a drain.

The main configuration of the invention is in that in the case in which impurities are ion implanted into a semiconductor substrate made of Si single crystal to form impurity extension regions, and thereafter an annealing treatment is performed on the substrate to activate the impurities so as to form a source and a drain, the source and the drain are preferably formed using laser annealing for the annealing treatment.

Specifically, as shown in Fig. 1, a gate electrode 3 is pattern formed above a semiconductor substrate 1 made of n-type silicon single crystal through a gate insulating film 2. Thereafter, atoms, Ge^+ in this example, having properties just enough to amorphize single crystal Si are ion implanted (shown by arrows 4) from oblique directions to the Si surface of the substrate 1 with the gate electrode 3 as a mask to melt and re-crystallize the single crystal Si so as to form amorphous regions 5 which seep into the substrate 1 under the gate electrode 3.

Thereafter p-type impurities, B^+ in this example, are ion implanted into the amorphous regions 5 and laser irradiation is executed thereon. Incidentally, the Ge implanting step and the B implanting step may be executed with their sequence changed.

Fig. 2 shows results of secondary ion mass spectrometry of samples to which the Ge implantation and the B implantation are executed and then the laser annealing is performed.

The ion implantation of atoms having a large mass such as Ge, Si and As amorphizes the Si substrate. The region which has been amorphized has a melting point lower than that of the single crystal region. Therefore, a region to be melted by the laser irradiation can be controlled by selecting the laser irradiation condition, adjusting the depth of the amorphous region by selecting acceleration energy for the ion implantation here, and by selecting the laser irradiation condition to melt the amorphous region and not to melt the single crystal region.

Fig. 2 shows the results of the samples of which the depths of the amorphous regions are varied by changing the acceleration energy at the time of Ge implanting. The implantation of heavy atoms in an oblique direction also enables control of the region to be melted in the horizontal direction. This technique is employed at the time of implanting impurities after the formation of the gate electrode,

which enables control of the amorphous region which seeps into under the gate electrode. Before or after the step of ion implanting the heavy atoms, impurities for forming a pn junction are ion implanted and the laser annealing is performed thereon, which makes it possible to control the amount of overlap between the impurity extension region and the gate.

Further, when this technique is combined with the process of fabricating a MOS transistor having a metal (Al, Cu or the like) gate electrode, there is an advantage that the metal gate electrode is not susceptible to a damage by the ion implantation of heavy atoms as compared to a polysilicon gate electrode.

Furthermore, when a combination of a gate insulating film composed of a high-dielectric insulating film such as tantalumoxide and a metal gate electrode is employed, only the source and the drain which actually need to be heat treated can be selectively heat treated while the gate insulating film is not influenced by heat in the laser annealing process. Therefore, it is possible to improve compatibility with the MOS transistor process of the high-dielectric insulating film which dislikes a heat treatment at high temperatures.

Moreover, instead of implanting into the Si surface of the substrate 1 from the oblique

directions the atoms having properties just enough to amorphize the single crystal Si as described above, the atoms are vertically implanted into the Si surface as in the normal case as shown in Fig. 3. In this case it is also possible to form a source and a drain 6 having parts corresponding to the amorphous regions 5 which seep into the substrate 1 under the gate electrode 3 by controlling a condition of introducing the atoms (Ge^+) and a condition of intensity of the laser irradiation respectively.

In other words, in this case, the fact is utilized that the substrate becomes amorphous by implanting the atoms having a large mass such as Ge, Si and As and the region which has become amorphous has a melting point lower than that of the single crystal region as described above. The condition of introducing the atoms shall be a condition enough for the amorphous regions to seep into the substrate 1 under the gate electrode 3 by adjusting the depth of the amorphous regions, and the condition of intensity of the laser irradiation shall be a condition that the amorphous regions melt but the single crystal region does not melt. This enables control of the regions to be melted by the laser irradiation. In this event, not only extension of dopant such as B^+ in the depth direction changes as in Fig. 2 but also extension of dopant seeping into under the gate electrode 3 changes (Fig. 4 shows the overlapping

length between a lower part of the gate electrode 3 and the source and the drain 6 in Fig. 2). The extension can also be controlled by the intensity of the laser irradiation. More specifically, by adjusting the ion implantation energy of the heavy atoms, the extension of the amorphous regions can be adjusted not only in the depth direction but also in the horizontal direction. Therefore, it becomes possible to control the extension in the horizontal direction of the dopant into under the gate electrode 3 by the combination with the adjustment of the intensity of the laser irradiation.

-Concrete embodiments-

Hereafter, concrete embodiments of a method of manufacturing a MOS transistor to which the present invention is applied will be described.

-First Embodiment-

First, the first embodiment is explained in order of step using Figs. 5A to 5E and Figs. 6A to 6C.

(1) From element isolation to gate electrode formation (Fig. 5A)

First, on a semiconductor substrate 11 made of single crystal Si, normal process of manufacturing a MOS transistor is executed which includes the formation of a not shown element isolation structure for defining an element region (a field oxide film by the LOCOS method, a local insulating film by the STI method and so on), the formation of a well structure

by ion implantation of impurities, ion implantation for controlling the threshold value and so on.

Then, a gate insulating film 12 is formed on the defined element region of the semiconductor substrate 11. This gate insulating film is of one type selected from among a silicon oxide film, a silicon nitride film, a silicon oxynitride film and a metal oxide film having a dielectric constant higher than that of the silicon oxide film, or of a film having a laminated structure thereof.

Subsequently, a gate electrode material, one type selected from among polysilicon, poly-germanium, polysilicon-germanium, and metals such as Al, Cu and so on here is deposited on the gate insulating film 12. The electrode material and the gate insulating film 12 are patterned by photolithography and subsequent dry etching to form a gate electrode 13 (and the gate insulating film 12 processed in the shape following it).

(2) Formation of first amorphous regions by ion implantation using heavy atoms (Fig. 5B)

Atoms having properties just enough to amorphize single crystal Si are ion implanted (shown by arrows A1) from oblique directions to a surface layer of the element region of the semiconductor substrate 11 with the gate electrode 13 as a mask. As the atoms, one element selected from among Si, Ge, As and Ar is preferable. The atoms here shall be Ge^+, and the

implantation conditions shall be 15 keV of acceleration energy and $4 \times 10^{14}/cm^2$ of dose. Further, the directions of the ion implantation shall be tilt 20 with an angle x° from a direction vertical to the surface of the semiconductor substrate 11 being defined as tilt x (i.e., the vertical direction is tilt 0). The single crystal Si is melted and re-crystallized by this ion implantation to form first amorphous regions 14 such as to seep into the substrate 11 under the gate electrode 13.

(3) Formation of shallow pn junctions (Fig. 5C)

Subsequently, impurities having a conductive type opposite to that of the semiconductor substrate 11 are ion implanted (shown by arrows A2) into the surface layer of the element region with the gate electrode 13 as a mask. For example, if the MOS transistor to be manufactured is a PMOS as shown in Fig. 5C, B^+ ions are implanted under conditions of 0.5 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose, and if the MOS transistor to be manufactured is an NMOS, P^+ ions are implanted under conditions of 2 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose, so as to form shallow pn junction regions 15.

(4) Formation of second amorphous regions by ion implantation using heavy atoms (Fig. 5D)

Subsequently, an insulating film such as a silicon oxide film, a silicon nitride film or the like is formed by deposition on the entire surface of

the substrate. Thereafter the entire surface of this insulating film is subjected to anisotropic etching (etch back) to thereby form side walls 16 with the insulating film left only on the side surfaces of the gate electrode 13.

Subsequently, atoms having properties just enough to amorphize single crystal Si, Ge^+ here, are ion implanted (shown by arrows A3) into the surface layers of the element regions with the gate electrode 13 and the side walls 16 as a mask to form second amorphous regions 17. In this event, the implantation conditions shall be conditions for amorphousizing the regions deeper than at time of forming the first amorphous regions 14, for example, 60 keV of acceleration energy and $4 \times 10^{14}/cm^2$ of dose.

(5) Formation of deep pn junctions (Fig. 5E)

Subsequently, impurities having a conductive type opposite to that of the semiconductor substrate 11 are ion implanted (shown by arrows A4) into the surface layers of the element regions with the gate electrode 13 and the side walls 16 as a mask. In this event, the implantation conditions shall be conditions for extending the impurities deeper than at the time of forming the shallow pn junction regions 15. For example, if the MOS transistor to be manufactured is a PMOS as shown in Fig. 5E, B^+ ions are implanted under conditions of 5 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose, and if

the MOS transistor to be manufactured is an NMOS, P^+ ions are implanted under conditions of 15 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose, so as to form deep pn junction regions 18 which are superposed on the shallow pn junction regions 15.

(6) Laser annealing (Fig. 6A)

Subsequently, the side walls 16 are removed by wet etching using hydrofluoric acid, and thereafter the substrate surface is irradiated with excimer pulse laser of XeCl, ArF or the like one or a plural times (shown by arrows A5) to activate the impurities in the pn junction regions 15 and 18, so as to form a source and a drain 19 corresponding to the pn junction regions 15 and 18.

As described above, in this example, the source and the drain 19 of an LDD structure composed of two types of junction regions can be activated in one laser annealing step. The formed a source and a drain 19 have a capacitance on the source side of 0.25 (fF/μm/side) or more. This capacitance is an index showing the amount of overlap between the source and the drain and the gate electrode. The capacitance is about 0.20 fF/μm in the conventional MOS transistor using the laser annealing method, but a capacitance of 0.25 (fF/μm/side) or more is secured in this embodiment, and thus it is conceivable that enough overlap is obtained.

(7) Silicidation (Salicidation) (Fig. 6B or Fig. 6C)

First, an insulating film such as a silicon oxide film, a silicon nitride film or the like is formed by deposition on the entire surface of the substrate. Thereafter the entire surface of this insulating film is subjected to anisotropic etching (etch back) to thereby form again side walls 20 with the insulating film left only on the side surfaces of the gate electrode 13.

Subsequently, as shown in Fig. 6B, when the gate electrode 13 is a metal gate made of a metal material such as Al, Cu or the like, a metal film such as Ti, Pt, Co, Ni or the like is formed on the source and the drain 19 by the sputtering method or the like and is subjected to an annealing treatment as a siliciding process to form metal silicide films 21.

On the other hand, as shown in Fig. 6C, when the gate electrode 13 is made of polysilicon or the like, a metal film such as Ti, Pt, Co, Ni or the like is formed on the gate electrode 13 and the source and the drain 19 by the sputtering method or the like and is subjected to an annealing treatment as a saliciding process to form metal silicide films 21.

The source and the drain 19 which have been activated and formed by the laser annealing have good compatibility with the siliciding (saliciding) process because of their box-shape impurity profiles which are activated to have a high impurity concentration.

Thereafter, through the following process such as the formation of a not shown interlayer insulating film, a contact hole and each wiring layer, the MOS transistor is completed.

As described above, according to this embodiment, it becomes possible to obtain a sharp impurity profile through the use of the laser annealing method without presenting a disadvantage such as an increase in parasitic resistance or the like to thereby meet sufficiently the requirements for making a MOS transistor finer and more highly integrated.

It should be noted that the MOS transistor is illustrated as a semiconductor device, in which the main configuration of the present invention is applied to the laser annealing treatment in forming the source and the drain of the LDD structure in this embodiment. The present invention, however, is not limited to this, but is also preferably applied to, for example, the case in which three times or more of impurity ion implantation are required under different introduction conditions, heavy atom ion implantation is performed for amorphousization in correspondence with each impurity ion implantation, and the impurities are activated in one laser annealing treatment.

-Second Embodiment-

Next, the second embodiment is explained in order of step using Figs. 7A to 7D.

(1) From element isolation to gate electrode formation (Fig. 7A)

First, on a semiconductor substrate 11 made of single crystal Si, normal process of manufacturing a MOS transistor is executed which includes the formation of a not shown element isolation structure for defining an element region (a field oxide film by the LOCOS method, a local insulating film by the STI method and so on), the formation of a well structure by ion implantation of impurities, ion implantation for controlling the threshold value and so on.

Then, a gate insulating film 12 is formed on the defined element region of the semiconductor substrate 11. This gate insulating film is of one type selected from among a silicon oxide film, a silicon nitride film, a silicon oxynitride film and a metal oxide film having a dielectric constant higher than that of the silicon oxide film, or of a film having a laminated structure thereof.

Subsequently, a gate electrode material, one type selected from among polysilicon, poly-germanium, polysilicon-germanium, and metals such as Al, Cu and so on here is deposited on the gate insulating film 12. The electrode material and the gate insulating film 12 are patterned by photolithography and subsequent dry etching to form a gate electrode 13 (and the gate insulating film 12 processed in the shape following it).

(2) Formation of amorphous regions by ion implantation using heavy atoms (Fig. 7B)

Atoms having properties just enough to amorphize single crystal Si are ion implanted (shown by arrows A1) from oblique directions to surface layer of the element region of the substrate 11 with the gate electrode 13 as a mask. As the atoms, one element selected from among Si, Ge, As and Ar is preferable. The atoms here shall be Ge^+, and the implantation conditions shall be 15 keV of acceleration energy and $4 \times 10^{14}/cm^2$ of dose.

In this embodiment, the tilt angles of the introduction of atoms with respect to a direction vertical to the surface of the semiconductor substrate 11 are controlled so as to be greater on the source side S than on the drain side D. Thereby, the amorphous regions are formed such that the amount of seeping into the semiconductor substrate 11 under the gate electrode 13 is greater on the source side S than on the drain side D. Specifically, the directions of the ion implantation shall be tilt 0 on the drain side D and tilt 30 on the source side S with an angle x° from the direction vertical to the surface of the semiconductor substrate 11 being defined as tilt x (i.e., the vertical direction is tilt 0). By this ion implantation, the single crystal Si on the drain side D is melted and re-crystallized to form an amorphous region 31b such as

to seep into the substrate 11 under the gate electrode 13. On the source side S, an amorphous region 31a is formed which has an amount of seeping greater than that of the amorphous region 31b.

(3) Formation of a source and a drain (Fig. 7C)

Subsequently, impurities having a conductive type opposite to that of the semiconductor substrate 11 are ion implanted (shown by arrows A2) into the surface layer of the element region with the gate electrode 13 as a mask. For example, if the MOS transistor to be manufactured is a PMOS as shown in Fig. 7C, B^+ ions are implanted under conditions of 0.5 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose, and if the MOS transistor to be manufactured is an NMOS, As^+ ions are implanted under conditions of 2 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose, so as to form a pn junction region 32b on the drain side D and a pn junction region 32a on the source side S.

(4) Laser annealing (Fig. 7D)

First, a heat absorbing film is formed to cover the gate electrode 13. This heat absorbing film is constituted by forming a silicon oxide film 33a by the CVD method to have a film thickness of 5 nm to 50 nm and further forming a TaN film 33b by the sputtering method to have a film thickness of 20 nm to 40 nm.

Subsequently, the substrate surface is irradiated with excimer pulse laser of XeCl, ArF or the like, or

laser beams using YAG laser or the like one or a plural times (shown by arrows A3) to activate the impurities in the pn junction regions 32a and 32b, so as to form a source 33 and a drain 34 corresponding to the pn junction regions 32a and 32b. In this case, the laser power is selected from a range from 0.1 (J/cm^2) to 0.4 (J/cm^2).

As described above, in this embodiment, the amorphous regions 31 seeping into under the gate electrode 13 are controlled to be greater on the source side than that on the drain side. This makes it possible to make large the amount of overlap on the source side having great effect of suppressing parasitic resistance and to make small the amount of overlap on the drain side for suppressing the short channel effect.

As for the source 33 and the drain 34, the capacitance on the source side is 0.25 ($fF/\mu m$/side) or more. This capacitance is an index showing the amount of overlap between the source and the drain and the gate electrode. The capacitance is about 0.20 $fF/\mu m$ in the conventional MOS transistor using the laser annealing method, but a capacitance of 0.25 ($fF/\mu m$/side) or more is secured in this embodiment, and thus it is conceivable that enough overlap is obtained.

As described above, according to this embodiment, it becomes possible to obtain a sharp impurity

profile through the use of the laser annealing method without presenting a disadvantage such as an increase in parasitic resistance or the like to thereby meet sufficiently the requirements for making a MOS transistor finer and more highly integrated.

-Third Embodiment-

Next, the third embodiment is explained in order of step using Figs. 8A to 8D.

(1) From element isolation to gate electrode formation (Fig. 8A)

First, on a semiconductor substrate 11 made of single crystal Si, normal process of manufacturing a MOS transistor is executed which includes the formation of a not shown element isolation structure for defining an element region (a field oxide film by the LOCOS method, a local insulating film by the STI method and so on), the formation of a well structure by ion implantation of impurities, ion implantation for controlling the threshold value and so on.

Then, a gate insulating film 12 is formed on the defined element region of the semiconductor substrate 11. This gate insulating film is of one type selected from among a silicon oxide film, a silicon nitride film, a silicon oxynitride film and a metal oxide film having a dielectric constant higher than that of the silicon oxide film, or of a film having a laminated structure thereof.

Subsequently, a gate electrode material, one type selected from among polysilicon, poly-germanium, polysilicon-germanium, and metals such as Al, Cu and so on here is deposited on the gate insulating film 12. The electrode material and the gate insulating film 12 are patterned by photolithography and subsequent dry etching to form a gate electrode 13 (and the gate insulating film 12 processed in the shape following it).

(2) Formation of amorphous regions by ion implantation using heavy atoms (Fig. 8B)

Atoms having properties just enough to amorphize single crystal Si are ion implanted (shown by arrows A1) from oblique directions to a surface layer of the element region of the substrate 11 with the gate electrode 13 as a mask. The ion implantation is controlled so that the extension length in the depth direction is 20 nm to 60 nm and the extension length in the horizontal direction is 10 nm to 30 nm to form amorphous regions 41. As the atoms, one element selected from among Si, Ge, As and Ar is preferable. The atoms here shall be Ge^+, and the implantation conditions shall be 15 keV of acceleration energy and $4 \times 10^{14}/cm^2$ of dose.

(3) Formation of a source and a drain (Fig. 8C)

Subsequently, impurities having a conductive type opposite to that of the semiconductor substrate 11 are ion implanted (shown by arrows A2) into the

surface layer of the element region with the gate electrode 13 as a mask. For example, if the MOS transistor to be manufactured is a PMOS as shown in Fig. 8C, B^+ ions are implanted under conditions of 0.5 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose, and if the MOS transistor to be manufactured is an NMOS, As^+ ions are implanted under conditions of 5 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose, so as to form pn junction regions 42.

(4) Laser annealing (Fig. 8D)

First, a heat absorbing film is formed to cover the gate electrode 13. The heat absorbing film is constituted by forming a silicon oxide film 33a by the CVD method to have a film thickness of 5 nm to 50 nm and further forming a TaN film 33b by the sputtering method to have a film thickness of 20 nm to 40 nm.

Subsequently, the substrate surface is irradiated with excimer pulse laser of XeCl, ArF or the like, or laser beams using YAG laser or the like one or a plural times (shown by arrows A3) to activate the impurities in the pn junction regions 42, so as to form a source and a drain 19 corresponding to the pn junction regions 42. In this case, the laser power is selected from a range from 0.1 (J/cm^2) to 0.4 (J/cm^2).

As described above, in this example, the formed a source and a drain 19 have a capacitance on the

source side of 0.25 (fF/μm/side) or more. This capacitance is an index showing the amount of overlap between the source and the drain and the gate electrode. The capacitance is about 0.20 (fF/μm/side) in the conventional MOS transistor using the laser annealing method, but a capacitance of 0.25 (fF/μm/side) or more is secured in this embodiment, and thus it is conceivable that enough overlap is obtained.

As described above, according to this embodiment, it becomes possible to obtain a sharp impurity profile through the use of the laser annealing method without presenting a disadvantage such as an increase in parasitic resistance or the like to thereby meet sufficiently the requirements for making a MOS transistor finer and more highly integrated.

-Modified examples-

Modified examples of the third embodiment are explained here. These modified examples illustrate CMOS transistors of an LDD structure.

(Modified example 1)

First, the modified example 1 is explained in order of step using Figs. 9A to 9E.

(1) From element isolation to formation of gate electrodes and deep pn junctions (Fig. 9A)

First, on a semiconductor substrate 11 made of single crystal Si, normal process of manufacturing a MOS transistor is executed which includes the

formation of not shown element isolation structures for defining element regions (a field oxide film by the LOCOS method, a local insulating film by the STI method and so on), the formation of well structures by ion implantation of impurities, ion implantation for controlling the threshold value and so on.

Then, a gate insulating film 12 is formed on the defined element regions of the semiconductor substrate 11. This gate insulating film is of one type selected from among a silicon oxide film, a silicon nitride film, a silicon oxynitride film and a metal oxide film having a dielectric constant higher than that of the silicon oxide film, or of a film having a laminated structure thereof.

Subsequently, a gate electrode material, one type selected from among polysilicon, poly-germanium, polysilicon-germanium, and metals such as Al, Cu and so on here is deposited on the gate insulating film 12. The electrode material and the gate insulating film 12 are patterned by photolithography and subsequent dry etching to form gate electrodes 13 (and the gate insulating films 12 processed in the shape following them).

(2) Formation of shallow amorphous regions by ion implantation using heavy atoms

Atoms having properties just enough to amorphize single crystal Si are ion implanted (shown by arrows A1) into surface layers of the element regions of the

substrate 11 with the gate electrodes 13 as a mask. The ion implantation is controlled so that the extension length in the depth direction is 20 nm to 60 nm and the extension length in the horizontal direction is 10 nm to 30 nm so as to form shallow amorphous regions 51. The impurity distribution after the later-described laser annealing step is determined by the extension of the shallow amorphous regions 51. This extension is determined by the aforesaid ion implantation conditions of the atoms as described above. As the atoms, one element selected from among Si, Ge, As and Ar is preferable. The atoms here shall be Ge^+, and the implantation conditions shall be 10 keV to 60 keV of acceleration energy and $4 \times 10^{14}/cm^2$ of dose.

(3) Formation of deep amorphous regions by ion implantation using heavy atoms (Fig. 9B)

An insulating film such as a silicon oxide film, a silicon nitride film or the like is formed by deposition on the entire surface of the substrate. Thereafter the entire surface of this insulating film is subjected to anisotropic etching (etch back) to thereby form side walls 16 with the insulating film left only on the side surfaces of the gate electrodes 13.

Subsequently, atoms having properties just enough to amorphize single crystal Si are ion implanted (shown by arrows A2) into the surface layers of the

element regions of the semiconductor substrate 11 with the gate electrodes 13 and the side walls 16 as a mask. The ion implantation is controlled so that the extension length in the depth direction is 50 nm to 70 nm so as to form deep amorphous regions 52 to be connected to the amorphous regions 51. The impurity distribution after the later-described laser annealing step is determined by the extension of the amorphous regions 52. This extension is determined by the ion implantation conditions of the aforesaid atoms as described above. As the atoms, one element selected from among Si, Ge, As and Ar is preferable. The atoms here shall be Ge^+, and the implantation conditions shall be 40 keV to 80 keV of acceleration energy and $4 \times 10^{14}/cm^2$ of dose.

(4) Formation of pn junctions (Figs. 9C and 9D)

After the side walls 16 are removed, impurities having a conductive type opposite to that of the semiconductor substrate 11 are ion implanted (shown by arrows A3) into the surface layers of the element regions with the gate electrodes 13 as a mask. For example, when ion implantation is executed to an NMOS region as shown in Fig. 9C, for example, As^+ ions are implanted under conditions of 2 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose while a PMOS region is masked with a resist pattern 43. This forms n regions 53a which are pn junction regions. On the other hand, when ion implantation is executed to the

PMOS region, for example, B^+ ions are implanted under conditions of 0.5 keV of acceleration energy and 1 × $10^{16}/cm^2$ of dose while the NMOS region is masked with a resist pattern 44. This forms p regions 53b which are pn junction regions.

(5) Laser annealing (Fig. 9E)

Subsequently, the substrate surface is irradiated with excimer pulse laser of XeCl, ArF or the like under conditions of 0.3 (J/cm^2) of laser power one or a plural times (shown by arrows A4) to activate the impurities in the pn junction regions 53a and 53b, so as to form a source and a drain (n a source and a drain 19a and p a source and a drain 19b) corresponding to the pn junction regions 53a and 53b.

As described above, in this example, the source and the drain 19a and 19b of an LDD structure composed of two types of junction regions can be activated in one laser annealing step. The formed a source and a drain 19a and 19b have a capacitance on the source side of 0.25 (fF/μm/side) or more. This capacitance is an index showing the amount of overlap between the source and the drain and the gate electrode. The capacitance is about 0.20 fF/μm in the conventional MOS transistor using the laser annealing method, but a capacitance of 0.25 (fF/μm/side) or more is secured in this embodiment, and thus it is conceivable that enough overlap is obtained.

It should be noted that thereafter side walls may be formed again on the side surfaces of the gate electrodes 13 and may be silicided (salicided).

(Modified example 2)

Next, the modified example 2 is explained in order of step using Figs. 10A to 10E.

(1) From element isolation to formation of gate electrodes and deep pn junctions (Fig. 10A)

First, on a semiconductor substrate 11 made of single crystal Si, normal process of manufacturing a MOS transistor is executed which includes the formation of not shown element isolation structures for defining element regions (a field oxide film by the LOCOS method, a local insulating film by the STI method and so on), the formation of well structures by ion implantation of impurities, ion implantation for controlling the threshold value and so on.

Then, a gate insulating film 12 is formed on the defined element regions of the semiconductor substrate 11. This gate insulating film is of one type selected from among a silicon oxide film, a silicon nitride film, a silicon oxynitride film and a metal oxide film having a dielectric constant higher than that of the silicon oxide film, or of a film having a laminated structure thereof.

Subsequently, a gate electrode material, one type selected from among polysilicon, poly-germanium, polysilicon-germanium, and metals such as Al, Cu and

so on here is deposited on the gate insulating film 12. The electrode material and the gate insulating film 12 are patterned by photolithography and subsequent dry etching to form gate electrodes 13 (and the gate insulating films 12 processed in the shape following them).

Subsequent, an insulating film such as a silicon oxide film, a silicon nitride film or the like is formed by deposition on the entire surface of the substrate. Thereafter the entire surface of this insulating film is subjected to anisotropic etching (etch back) to thereby form side walls 16 with the insulating film left only on the side surfaces of the gate electrodes 13.

Subsequently, impurities having a conductive type opposite to that of the semiconductor substrate 11 are ion implanted into the surface layers of the element regions with the gate electrodes 13 and the side walls 16 as a mask. In this case, as for the implantation conditions of the NMOS region, for example, As^+ ions are implanted under conditions of 25 keV of acceleration energy and $8 \times 10^{15}/cm^2$ of dose, or P^+ ions are implanted under conditions of 7 keV of acceleration energy and $8 \times 10^{15}/cm^2$ of dose. Then, an annealing treatment is performed for 10 minutes at a temperature of 100℃ to form deep pn junction regions 18 (n^+ regions 18a and p^+ regions 18b).

(2) Formation of amorphous regions by ion implantation using heavy atoms (Fig. 10B)

After the side walls 16 are removed, atoms having properties just enough to amorphize single crystal Si are ion implanted (shown by arrows A1) into the surface layers of the element regions of the substrate 11 with the gate electrodes 13 as a mask. The ion implantation is controlled so that the extension length in the depth direction is 20 nm to 60 nm and the extension length in the horizontal direction is 10 nm to 30 nm so as to form amorphous regions 41. The impurity distribution after the later-described laser annealing step is determined by the extension of the shallow amorphous regions 41. This extension is determined by the aforesaid ion implantation conditions of the atoms as described above. As the atoms, one element selected from among Si, Ge, As and Ar is preferable. The atoms here shall be Ge^+, and the implantation conditions shall be 10 keV to 60 keV of acceleration energy and $4 \times 10^{14}/cm^2$ of dose.

(3) Formation of shallow pn junctions (Figs. 10C and 10D)

Subsequently, impurities having a conductive type opposite to that of the semiconductor substrate 11 are ion implanted (shown by arrows A2) into the surface layers of the element regions with the gate electrode 13 as a mask. For example, when ion

implantation is executed to an NMOS region as shown in Fig. 10C, for example, As^+ ions are implanted under conditions of 2 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose while a PMOS region is masked with a resist pattern 43. This forms n regions 15a which are shallow pn junction regions. On the other hand, when ion implantation is executed to the PMOS region, for example, B^+ ions are implanted under conditions of 0.5 keV of acceleration energy and $1 \times 10^{16}/cm^2$ of dose while the NMOS region is masked with a resist pattern 44. This forms p regions 15b which are shallow pn junction regions.

(4) Laser annealing (Fig. 10E)

Subsequently, the substrate surface is irradiated with excimer pulse laser of XeCl, ArF or the like under conditions of, for example, 0.3 (J/cm^2) of laser power one or a plural times (shown by arrows A3) to activate the impurities in the pn junction regions 15 and 18, so as to form a source and a drain (n a source and a drain 19a and p a source and a drain 19b) corresponding to the pn junction regions 15 and 18.

As described above, in this example, the source and the drain 19a and 19b of an LDD structure composed of two types of junction regions can be activated in one laser annealing step. The formed a source and a drain 19a and 19b have a capacitance on the source side of 0.25 ($fF/\mu m$/side) or more. This

capacitance is an index showing the amount of overlap between the source and the drain and the gate electrode. The capacitance is about 0.20 (fF/μm/side) in the conventional MOS transistor using the laser annealing method, but a capacitance of 0.25 (fF/μm/side) or more is secured in this embodiment, and thus it is conceivable that enough overlap is obtained.

It should be noted that thereafter side walls may be formed again on the side surfaces of the gate electrodes 13 and may be silicided (salicided).

Further, in the above-described second embodiment, a CMOS transistor of an LDD structure can be manufactured as in this modified example.

It becomes possible to obtain a sharp impurity profile through the use of the laser annealing method without presenting a disadvantage such as an increase in parasitic resistance or the like to thereby meet sufficiently the requirements for making a MOS transistor finer and more highly integrated.